Временные ограничения

Оглавление

The most common types of path categories include:
• Input paths
• Synchronous element to synchronous element paths
• Path specific exceptions
• Output Paths

Input Timing Constraints

System Synchronous Inputs

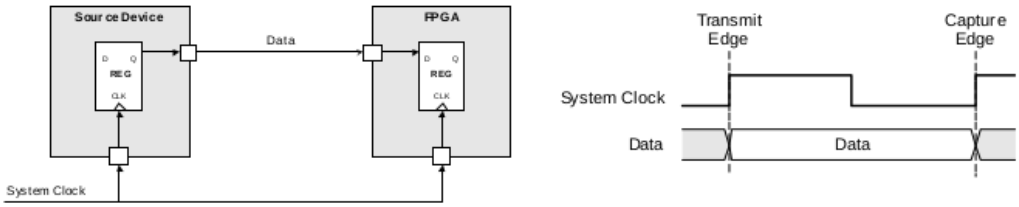
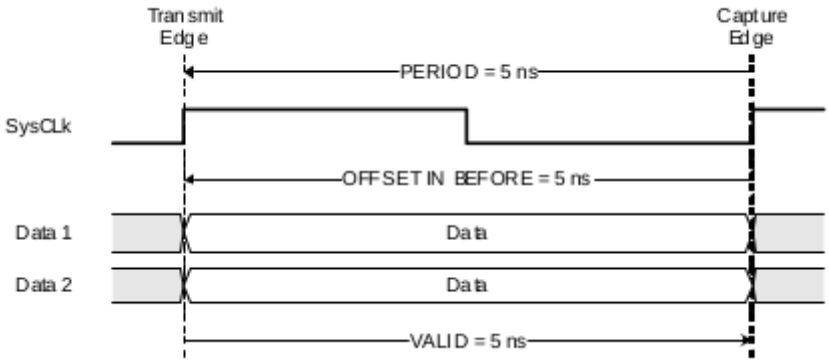


Figure 2-1: **Simplified System Synchronous interface with associated SDR timing**




```
NET "SysCLk" TNM_NET = "SysClk";
TIMESPEC "TS_SysClk" = PERIOD "SysClk" 5 ns HIGH 50%;
OFFSET = IN 5 ns VALID 5 ns BEFORE "SysClk";
```

Source Synchronous Inputs

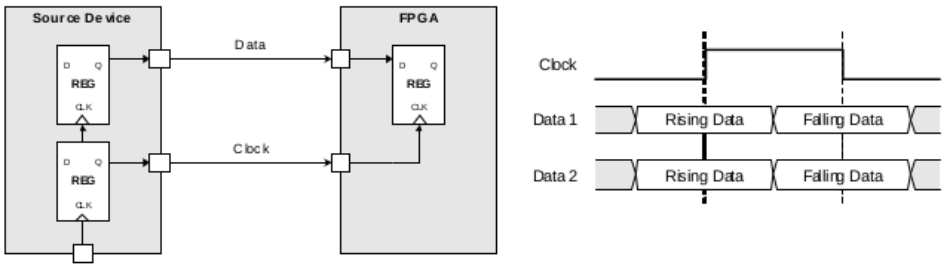
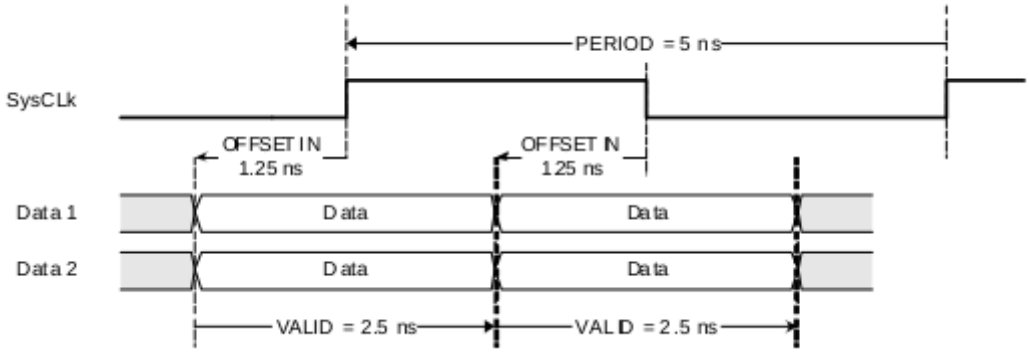


Figure 2-3: **Simplified Source Synchronous input interface with associated DDR timing**




```
NET "SysCLk" TNM_NET = "SysClk";
TIMESPEC "TS_SysClk" = PERIOD "SysClk" 5 ns HIGH 50%;
OFFSET = IN 1.25 ns VALID 2.5 ns BEFORE "SysClk" RISING;
OFFSET = IN 1.25 ns VALID 2.5 ns BEFORE "SysClk" FALLING;
```

Register-To-Register Timing Constraints

Automatically Related Synchronous DCM/PLL Clock Domains

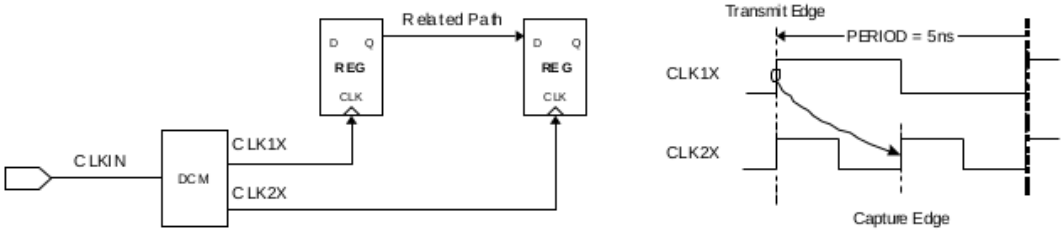


Figure 2-5: **The input clock of the design goes to a DCM example**

```
NET "ClkIn" TNM_NET = "ClkIn";
TIMESPEC "TS_ClkIn" = PERIOD "ClkIn" 5 ns HIGH 50%;
```

Manually Related Synchronous Clock Domains

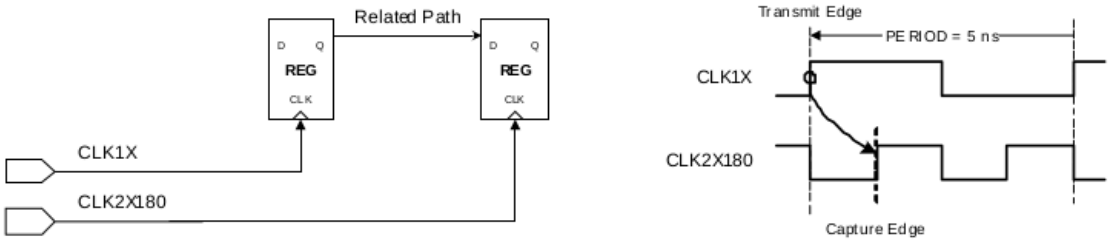


Figure 2-6: **Two related clocks entering the FPGA device through separate external pins**

```
NET "Clk1X" TNM_NET = "Clk1X";
NET "Clk2X180" TNM_NET = "Clk2X180";
TIMESPEC "TS_Clk1X" = PERIOD "Clk1X" 5 ns;
TIMESPEC "TS_Clk2X180" = PERIOD "Clk2X180" TS_Clk1X/2 PHASE + 1.25 ns ;
```

Asynchronous Clock Domains

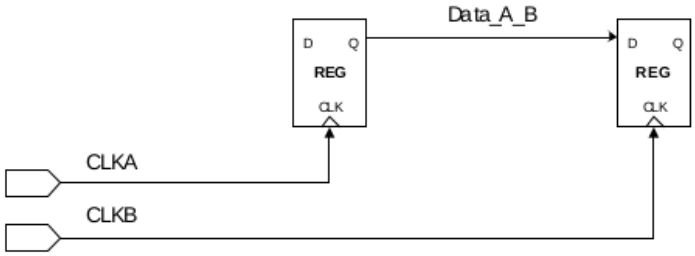


Figure 2-7: **Two unrelated clocks entering the FPGA device through separate external pins**

```
NET "CLKA" TNM_NET = FFS "GRP_A";
NET "CLKB" TNM_NET = FFS "GRP_B";
TIMESPEC TS_Example = FROM "GRP_A" TO "GRP_B" 5 ns DATAPATHONLY;
```

Output Timing Constraints

System Synchronous Output

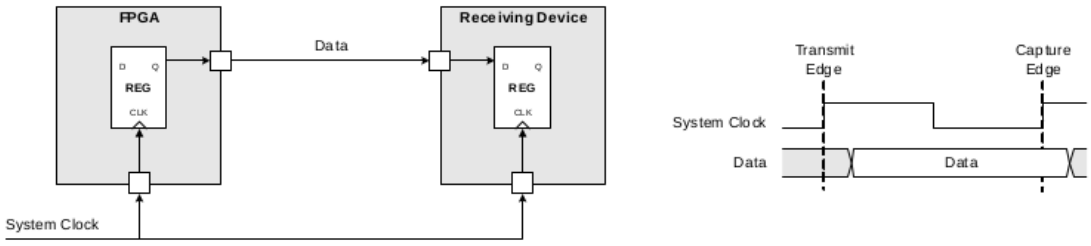


Figure 2-9: **Simplified System Synchronous output interface with associated SDR timing**

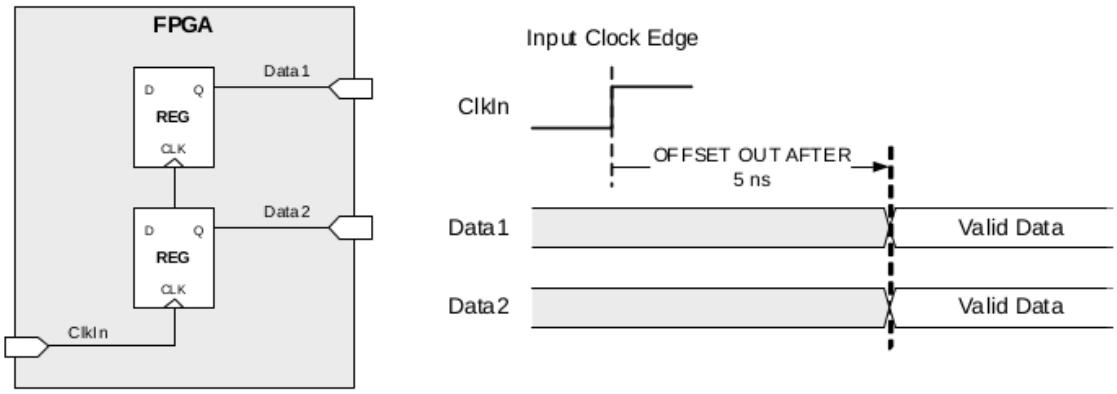


Figure 2-10: **Timing diagram for System Synchronous SDR output interface**

```
NET "ClkIn" TNM_NET = "ClkIn";
OFFSET = OUT 5 ns AFTER "ClkIn";
```

Source Synchronous Outputs

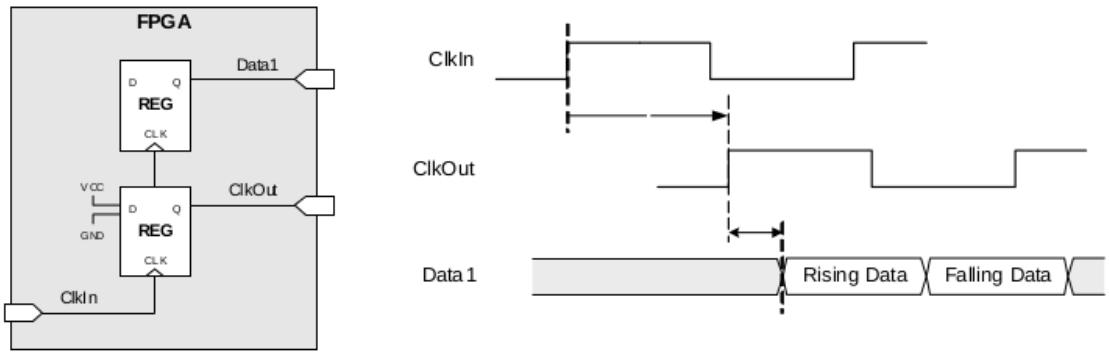


Figure 2-11: **Simplified Source Synchronous output interface with associated DDR timing**

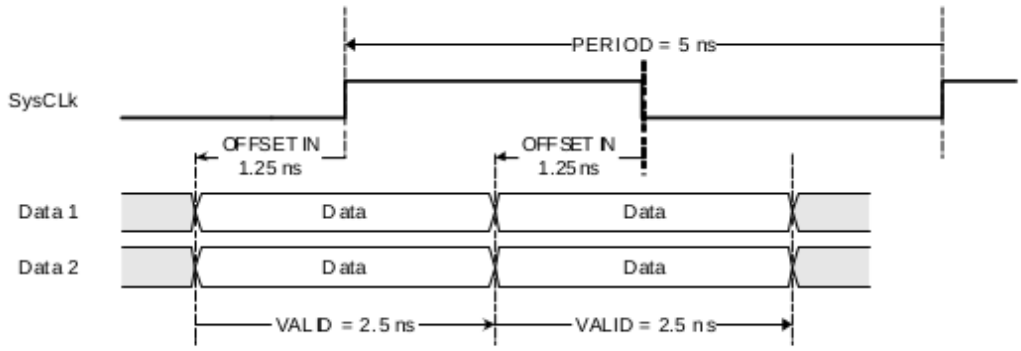


Figure 2-12: **Timing diagram for an ideal Source Synchronous DDR**

```
NET "SysCLk" TNM_NET = "SysClk";
TIMESPEC "TS_SysClk" = PERIOD "SysClk" 5 ns HIGH 50%;
OFFSET = IN 1.25 ns VALID 2.5 ns BEFORE "SysClk" RISING;
```

OFFSET = IN 1.25 ns VALID 2.5 ns BEFORE "SysClk" FALLING;

Timing Exceptions

False Paths

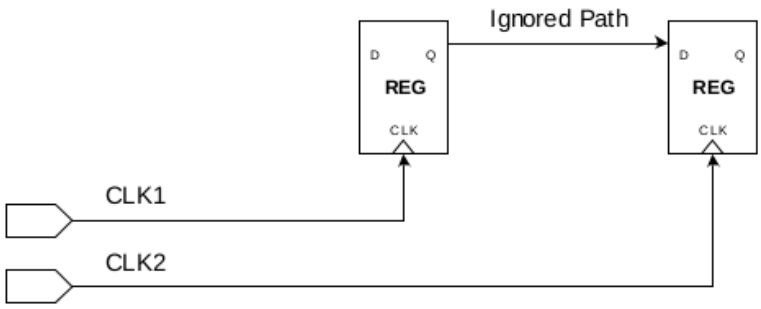


Figure 2-13: **Path between two registers that does not affect the timing of the design**

NET "CLK1" TNM_NET = FFS "GRP_1";
NET "CLK2" TNM_NET = FFS "GRP_2";
TIMESPEC TS_Example = FROM "GRP_1" TO "GRP_2" TIG;

Multi-Cycle Paths

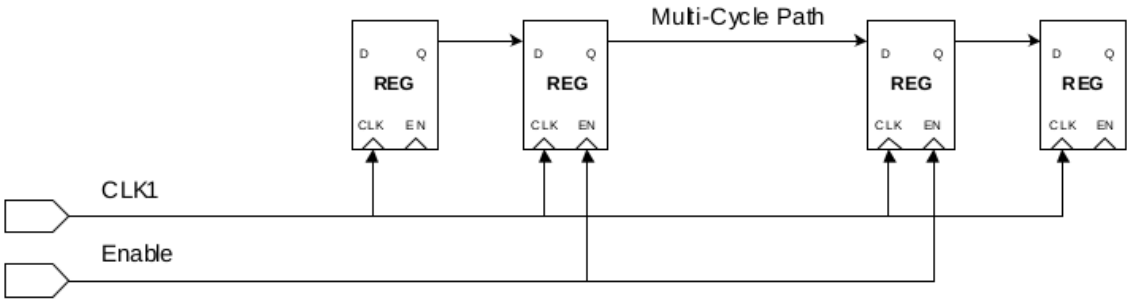


Figure 2-14: **Path between two registers clocked by a common clock enable signal**

NET "CLK1" TNM_NET = "CLK1";
TIMESPEC "TS_CLK1" = PERIOD "CLK1" 5 ns HIGH 50%;
NET "Enable" TNM_NET = FFS "MC_GRP";
TIMESPEC TS_Example = FROM "MC_GRP" TO "MC_GRP" TS_CLK1*2;